A NOVEL TEST STRUCTURE FOR SPEEDING A STRESS-INDUCED VOIDING TEST AND METHOD OF USING SAME

FIELD OF THE INVENTION

The present invention relates generally to testing and diagnostics of line processes used for the manufacture of integrated circuit devices and more specifically to the detection and measurement of voids in copper interconnect metallurgy.

BACKGROUND OF THE INVENTION

The manufacture of large scale integrated circuits in a mass production facility involves hundreds of discrete processing steps beginning with the introduction of blank semiconductor wafers at one end and recovering the completed chips at the other end. The manufacturing process is usually conceived as consisting of the segment wherein the semiconductor devices are formed within the silicon surface (front-end-of-line) and the portion which includes the formation of the various layers of interconnection metallurgy above the silicon surface (back-end-of-line). Most of these processing steps involve depositing layers of material, patterning them by photolithographic techniques and etching away the unwanted portions. These materials consist primarily of insulators and metal alloys.

In order to monitor the integrated circuit manufacturing process, test structures that are representative of the circuit elements are typically incorporated into regions of the wafer outside of the integrated circuit chips as product failures are closely correlated to test structure/site failures.

Examples of these in-line test devices are: a dumb-bell structure testable with a four point probe to establish proper resistivity of a deposited layer; or long serpentine metal lines which can be tested to establish the presence of particulate defects by testing for electrical opens and shorts. These devices are

typically designed with critical areas much larger than their corresponding elements in the integrated circuit so they are more sensitive to defects and can be tested at various stages during processing. In addition to such devices which characterize the cleanliness and integrity of the process line, test sites must also be provided which can characterize the integrity of pattern alignment and planar dimensions.

Of particular interest is this invention is the ability to detect the formation of voids in buried (copper) interconnect lines. These voids are typically created by mechanical stresses which cause delamination of the metal line from the adjacent insulative matrix. The resulting void, while not directly producing an open circuit in the metal line, is nevertheless responsible for creating a hot spot when a current is passed through the line. Such hot spots encourage electromigration in the copper which in turn causes migration of the void along the line, eventually combining with other voids to form a larger void at a point where the metal lines meet a contact or via. The result is an "open" failure. It would therefore be desirable to have a means of early detection of hidden stress induced voids in metal lines.

Traditional test structures use the copper (Cu) volume effect (where more volume causes more micro-vacancies produced after baking) to dominate the SIV failure only.

U.S. Patent No. 6,037,795 to Filippi et al. describes a multiple device test layout.

U.S. Patent No. 6,191,481 to Bothra et al. describes electromigration impeding composite metallization lines and methods for making the same.

U.S. Patent No. 5,973,402 to Shinriki et al. describes a metal interconnection and a method for making the same.

U.S. Patent No. 5,504,017 to Yue et al. describes void detection in metallization patterns.

U.S. Patent No. 5,156,909 to Henager, Jr. et al. describes thick, low-stress films, and coated substrates formed therefrom, and methods for making same.

U.S. Patent No. 5,010,024 to Allen et al. describes passivation for integrated circuit structures.

U.S. Patent Nos. 6,174,743 B1 and 6,221,794 B1, both to Pangrie et al., describe a method of reducing incidence of stress-induced voiding in semiconductor interconnect lines.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide a novel test structure for speeding the stress-induced voiding test.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a test structure, has: (1) a first member having: a roughly a rectangular shape; a first width dimension; and a first length dimension that is greater than the first width dimension; and (2) a second member having: a roughly a rectangular shape; a second width dimension; and a second length dimension that is greater than the second width dimension combined with the first member to form a roughly symmetrical cross-shaped test structure. Also a method of using the test structure to test for voids.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Fig. 1 is a top or bottom down plan view of a test structure known to the inventor showing stress contour simulation.

Fig. 2 is a top or bottom down plan view of the preferred embodiment test structure of the present invention showing stress contour simulation.

Fig. 3 is a graph showing relative failure rate by length/width/length.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Structure Known to the Inventor - Not to be Considered Prior Art - Fig. 1

Fig. 1 illustrates a structure known to the inventor and is not to be considered prior art for the purposes of this invention.

Fig. 1 illustrates a test structure 10 known to the inventor having a square shape with the dimensions 2X by 2X that utilizes the volume effect to dominate the Stress-Induced Voiding (SIV) failure only. Included in Fig. 1 is a stress contour simulation using finite elements analysis (FEA) showing stress gradients 12, 14, 16. Two metal lines 18, 20 intersect at about a 90° angle with a via 22 connecting their 18, 20 intersection with the approximate center 24 of the square-shaped test pattern 10.

Test Structure of the Present Invention - Fig. 2

Fig. 2 illustrates the cross-shaped test structure 100 of the present invention for speeding a stress-induced voiding test.

The inventor has discovered that the cross-shaped test structure 100 of the present invention can not only evaluate the volume effect, but can also utilize geometry-enhanced stress effect into consideration and thus this cross-shaped test structure 100 allows more strict examination than the traditional test structure of Fig. 1 for SIV and provides for the speeded-up testing so that the time to failure is reduced as the baking time may be reduced from about 500 hours for Fig. 1 to about 168 hours for Fig. 2 (also see below).

The cross-shaped test structure 100 may be formed on a special test wafer or on a test site or kerf on a product wafer. If formed upon a test wafer, the cross-shaped test structure 100 may be from about 0.4 X 0.4 μm to about 100.0 X 100.0μm.

The inventor has discovered that a test structure 100 having an area that is about 75% (3/4) of the area of the square-shaped test structure 10 known to the inventor and having a specific geometry, i.e. cross-shaped as shown in Fig. 2, accelerates SIV failure (Stress-Induced Voiding failure). Cross-shaped test structure 100 has a thickness of preferably from about 5000 to 10,000Å and more preferably about 5000Å. The cross-shaped test structure 100 is embedded and exposed within a dielectric layer formed over the silicon wafer.

Two metal lines 118, 120 intersect at about a 90° angle with a via 122 connecting their 118, 120 intersection with the approximate center 124 of the cross-shaped test pattern 100. Metal lines 118, 120 are formed within an inter-metal dielectric (IMD) layer formed over the dielectric layer with the via 122 extending from the cross-shaped test structure 100 to the metal line 118, 120 intersection. The via 122 having a cross-section of preferably from about 10^3 to 10^4Å^2.

Simply, the test structure 100, metal lines 118, 120 and via 122 are formed in the same way as is the product metallization, that is:

forming a dielectric layer over the silicon substrate/wafer/

forming a cross-shaped damascene opening within the dielectric layer;

filling the damascene opening with a first copper layer;

planarizing, preferably by chemical mechanical polishing (CMP), the copper layer to form the cross-shaped test structure 100;

forming an IMD layer over the planarized copper cross-shaped test structure 100 and the dielectric layer;

forming a dual damascene opening within the IMD layer with the lower via opening exposing a portion of the planarized cross-shaped test structure 100 approximate its center 124;

filling the dual damascene opening with a second copper layer; and

planarizing , preferably by chemical mechanical polishing (CMP), the second copper layer to form the via 122 and metal lines 118, 120.

Metal lines 118, 120 have a thickness of preferably from about 5000 to 10,000Å and more preferably about 5000Å. Via 122 has a length from the cross-shaped test structure 100 to the metal line 118, 120 intersection of preferably from about 5000 to 10,000Å and more preferably about 5000Å.

Graph of Relative Failure Rate by Length/Width/Length - Fig. 3

As shown in the graph of Fig. 3, the inventor has discovered that a maximum failure rate exits for a length (L) X width (W) X length (L) of 10X20X10, i.e. a rectangular dimension of X by 2X, using actual datum points despite the theoretical failure rate shown by the dashed line of Fig. 3.

Thus, the inventor combined two maximum failure X by 2X rectangular structures to form the maximum failure cross-shaped test structure 10 of the present invention shown in Fig. 2 having a total area that is about 75% (3/4) of the square-shaped test structure 10 known to the inventor and shown in Fig. 1.

Stress Contour Simulation Using FEA - Fig. 2

Also shown in Fig. 2, is a stress contour simulation using finite elements analysis (FEA) showing stress gradients 112, 114, 116, 117 exerting stresses 126 upon the approximate center 124 of the cross-shaped test structure 100 of the present invention proximate the connection to the via 122. Thus, the geometry-enhanced stress effect of the cross-shaped test structure 100 is also taken into consideration permitting a more strict examination of voiding.

The cross-shaped test structure 100 is thus enhances a maximum stress gradient (X by 2X).

These FEA simulations of Figs. 1 and 2 are strictly derived from a theoretical model of the test site using parameters such as thermal expansion coefficients and the thicknesses of the layers involved and use "Von Mises" stresses (equivalent stress).

Testing Procedure Utilizing the Cross-Shaped Test Structure 100

The resistance of the cross-shaped test structure 100, lines 118, 120 and via 122 is measured and then the entire structure 100, 118, 120, 122 is baked at from about 150 to 200°C for preferably from about greater than about 0 to 168 hours and more preferably about 168 hours and the resistance is again measured. Any voids formed in the cross-shaped test structure 100 are detected by the differences in the initial and post-baked resistance. Due to the geometry (that is cross-shaped)-enhanced stress effect as discussed above and illustrated by the stress contours in Fig. 2, the baking time can thus be dramatically reduced from about 500 hours needed for the structure of Fig. 1 known to the inventor to establish if any product failure occurred; to preferably from about 150 to 186 hours and more preferably about 168 hours for the cross-shaped test structure 100 of the present invention to establish if any product failure occurred.

While the written description of the present invention notes that the cross-shaped test structure 100, lines 118, 120 and via 124 are each more preferably comprised of copper (Cu).

Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. a test structure permitting quicker testing for voids; and
2. reducing the baking time in the voiding test.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.